Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL/MAY 2026

Fourth Semester

Biomedical Engineering

UBMT24402 – ANALOG AND DIGITAL INTEGRATED CIRCUITS

Regulations - 2024

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A(ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	Questions	BTL	CO	Marks
1.	What are all the characteristics of an ideal operational amplifier?	L1	1	2
2.	Define a function of Monostable Multivibrator?	L1	1	2
3.	Define sample and hold circuit?	L1	2	2
4.	Define resolution of ADC circuit	L1	2	2
5.	Convert the number (65784) into hexadecimal?	L2	3	2
6.	Implement a OR logic gate using an universal NAND gate?	L2	3	2
7.	Draw a circuit diagram of 2:1 Mux?	L1	4	2
8.	Distinguish between PAL and PLA?	L2	4	2
9.	Define Master/Slave FF?	L1	5	2
10.	Define universal shift register?	L1	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			Questions	BLT	CO	Marks
11.	a	i	Explain the working, operation, voltage gain and application for inverting and non-inverting amplifier circuit?	L2	1	10
		ii	Briefly explain about operational amplifier-based Differentiator?	L2	1	6
			Or			
	b	i	Explain the working of inverting and non-inverting based comparator with the block diagram and output waveform analysis?	L2	1	8
		ii	Drive the expression of output voltage, peak to peak output voltage and time period for triangular wave generator?	L4	1	8
12.	a	i	Write in detail about the function of inverted R-2R ladder DAC. If R = Rf = 10 kΩ and Vr=10V. Calculate the output voltage for the binary input of 101 with the consideration of inverted R-2R ladder DAC?	L3	2	10
		ii	Explain in detail about Successive approximation DAC.	L2	2	6
			Or			
	b	i	Explain the working of Voltage controlled Oscillator with the block diagram and output waveform analysis?	L2	2	10
		ii	Draw and explain the frequency Translator using PLL.	L2	2	6
13.	a	i	Convert $(10101011)_n$ into its equivalent Decimal, Octal, Hexadecimal.	L3	3	8
		ii	Reduce the following function using Karnaugh map technique. $F(A,B,C,D)=\pi M(0,3,4,7,8,10,12,14)+d(2,6)$	L4	3	8
			Or			
	b	i	Reduce the following function using Karnaugh map technique. $F(A,B,C,D)=\varepsilon M(5,6,7,12,13)+\varepsilon d(4,9,14,15)$	L4	3	8
		ii	Compare the logic families of TTL, MOS and CMOS.	L4	3	8

14.	a	i	Design a 4-bit Carry look ahead Adder using half adder and full adder circuit?	L4	4	8
		ii	Draw and explain the block diagram of n-bit parallel and binary adder subtractor.	L4	4	8
			Or			
	b	i	Design a 4-bit magnitude comparator with a circuit diagram using K-Map?	L4	4	8
		ii	Design a 3 to 8 Decoder using gates.	L4	4	8
15.	a	i	Explain right shift register using JK flip flop with block diagram in detail.	L2	5	8
		ii	Explain finite state machine with example	L4	5	8
			Or			
	b	i	Distinguish between synchronous and asynchronous sequential circuits.	L4	5	8
		ii	Explain synchronous decade using T flip-flop with block diagram in detail.	L2	5	8
